

ENGINEERING GRADUATE?

STUCK IN A NON-IT JOB?

Break into a Thriving Career in the VLSI Industry!

PROGRAM HIGHLIGHTS

Quick Completion V

24/7 Support

Proven Success >

Hands-On Training V



WHY CHOOSE US?

- QUICK COMPLETION: FINISH YOUR COURSE SWIFTLY AND EFFICIENTLY.
- 24/7 SUPPORT: GET HELP WHENEVER YOU NEED IT.
- PROVEN SUCCESS: JOIN OUR SUCCESSFUL ALUMNI IN THE VLSI INDUSTRY.
- HANDS-ON TRAINING: GAIN PRACTICAL, REAL-WORLD SKILLS.
- 100% PLACEMENT: SECURE A JOB UPON COMPLETION OF THE PROGRAM.





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APPLY NOW



VLSI DESIGN FLOW OVERVIEW

- REQUIREMENTS DEFINITION
- DESIGN SPECIFICATION & ARCHITECTURE
- RTL CODING
- RTL INTEGRATION
- FUNCTIONAL VERIFICATION
- SYNTHESIS
- DESIGN FOR TEST (DFT)
- PHYSICAL DESIGN
- STATIC TIMING ANALYSIS (STA)
- CUSTOM LAYOUT
- PHYSICAL VERIFICATION
- POST-SILICON VALIDATION

ESSENTIALS OF UNIX/LINUX

- LINUX/UNIX OPERATING SYSTEM
 AND SHELL
- WORKING WITH FILES AND DIRECTORIES
- COMMONLY USED COMMANDS

CMOS & FINFET BASICS

MOSFET BASICS, OPERATIONS, SIMPLE CIRCUITS, AND SECOND-ORDER EFFECTS

DETAILED FABRICATION PROCESS OF MOSFETS

FINFET WORKING PRINCIPLE, FABRICATION TECHNIQUES,
ADVANTAGES, AND DISADVANTAGES

CMOS & FINFET BASICS



CONDUCTOR, SEMICONDUCTOR, AND INSULATORS

- OVERVIEW OF THEIR PROPERTIES
 - DIFFERENCES BETWEEN INTRINSIC AND EXTRINSIC SEMICONDUCTORS



BASIC PASSIVE AND ACTIVE DEVICES

EXAMPLES OF EACH TYPE AND THEIR FUNCTIONS



OHM'S LAW AND KIRCHHOFF'S LAWS

PRINCIPLES AND APPLICATIONS IN CIRCUITS



FUNDAMENTALS OF CIRCUIT UNDERSTANDING

KEY CONCEPTS AND RELATIONSHIPS IN CIRCUIT ANALYSIS

LAYOUT TOOL ESSENTIALS

- LAYOUT EDITOR TOOL
- UNDERSTANDING THE SCHEMATIC SYMBOLS AND PARAMETERS
- CREATING AND MANAGING LIBRARIES AND CELLS
- COMMANDS FOR LAYOUT EDITING
- COMMANDS FOR SCHEMATIC EDITING
- VERIFICATION: DRC AND LVS

- ANTENNA EFFECT, LATCHUP, ELECTROMIGRATION, IR DROP
- ANALOG LAYOUT OF OPAMP, CURRENT MIRROR, ADC, AND DAC
- RESISTOR, CAPACITOR LAYOUT TECHNIQUES
- CMOS AND BICMOS LAYOUT TECHNIQUES
- STANDARD CELL LAYOUT: INVERTER, AND, OR, NAND, NOR, AOI, OAI, LATCHES, AND FLOP



ADVANCED LAYOUT CONCEPTS

- MISMATCHES & MATCHING
- FAILURE MECHANISMS: ELECTROMIGRATION, IR DROP, LOD & STRESS EFFECTS, WPE, ANTENNA EFFECTS, LATCH-UP, ESD (WITH HIGH VOLTAGE RULES, EOS EFFECTS)
- NOISES & COUPLING
- DIFFERENT TYPES OF PROCESSES ADVANTAGES & DISADVANTAGES:
 - PLANAR CMOS
 - FDSOI
 - SOI
 - BI-CMOS
 - GALLIUM ARSENIDE
 - SILICON-GERMANIUM
 - FINFET
- FULL CHIP CONSTRUCTION, SCRIBE SEAL, PAD FRAME, INTEGRATION, AND GUIDELINES
- PACKAGING

PHYSICAL VERIFICATION CONCEPTS

- DESIGN RULE CHECKS (DRC)
- LAYOUT VERSUS SCHEMATIC (LVS)
- ELECTRICAL RULE CHECKS (ERC)
- ANTENNA CHECKS
- (LATCH-UP
- RELIABILITY CHECKS LIKE EM AND IR ANALYSIS
- DESIGN FOR MANUFACTURABILITY (DFM) CHECKS

ANALOG AND MIXED SIGNAL LAYOUT

- HIGH-SPEED ANALOG LAYOUT
- HANDLING CLOCKS
- ANALOG CIRCUITS & LAYOUT GUIDELINES
- SINGLE & MULTI-STAGE DIFFERENTIAL OP-AMP LAYOUT
- CURRENT MIRROR LAYOUT
- PLL, DLL, AND OSCILLATORS
- LDO AND OTHER REGULATORS
- ADCS & DACS
- BANDGAP, TEMPERATURE SENSORS & BIASES: CURRENT & VOLTAGE BIAS LINES
- LARGE DRIVERS
- INPUT PAIR, DIFFERENTIAL ROUTING, POWER ROUTING, OFFSET MINIMIZING
- POWER/SIGNAL IR DROP
- CROSS-TALK AND COUPLING
- ELECTROSTATIC DISCHARGE (ESD)
- DEEP SUB-MICRON LAYOUT ISSUES
- SHALLOW TRENCH ISOLATION (STI)
- WELL PROXIMITY EFFECT (WPE)

ASSIGNMENTS AND HANDS-ON PROJECTS

ASSIGNMENTS AND MULTIPLE HANDS-ON PROJECTS

BEST PRACTICES & INTERVIEW QUESTIONS

BY THE END OF TRAINING STUDENTS WILL BE FAMILIAR WITH

COMPLETE LAYOUT FLOW INCLUDING

• FLOOR

PLANNING

- SCHEMATIC
- LAYOUT

AND ALSO

- STANDARD CELL LAYOUT OF DIGITAL GATES
- LEVEL SHIFTER
- SCHMITT TRIGGER
- SINGLE STAGE OP-AMP
- 4-BIT FLASH ADC
- 4-BIT DAC
- BANDGAP REFERENCE WITH START-UP CIRCUIT
- LOW DROP-OUT REGULATOR CIRCUIT

Trainee Engineers TESTIMONIAL









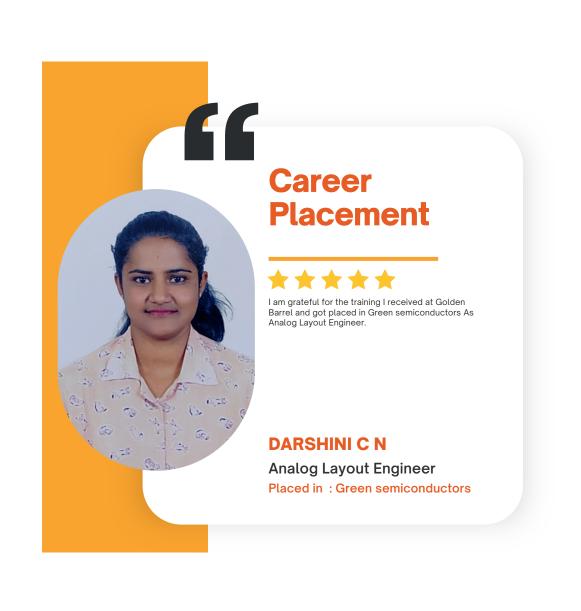






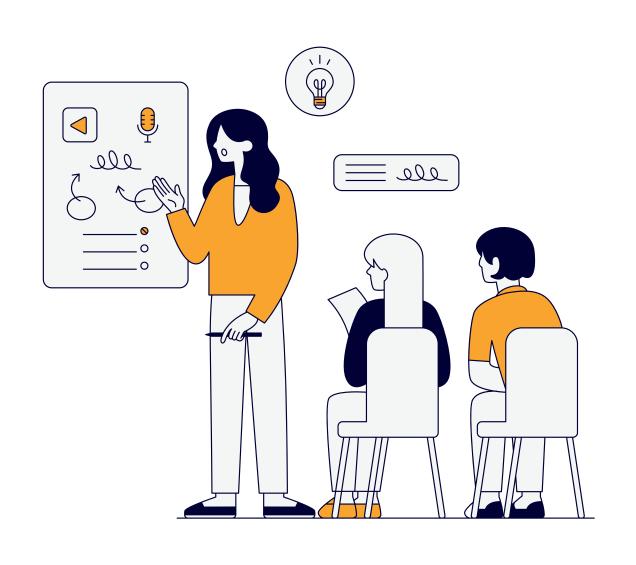












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